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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,170	05/05/2005	Keiji Mabuchi	09792909-6249	9957

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EXAMINER	
HSU, AMY R	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
06/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,170	MABUCHI, KEIJI	
	Examiner	Art Unit	
	AMY HSU	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,6-8 (renumbered as 1-7)* is/are allowed.

6)☒ Claim(s) *9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael Day on June 3, 2008.

The application has been amended as follows:

a. Claim 1 reads as follows:

A solid-state imaging apparatus comprising:

a pixel array, said pixel array comprising a plurality of pixels in a two-dimensional array;

a pixel-array scanning circuit that scans the pixel array to read analog signals from the individual pixels to an AD (analog to digital) memory,

the AD memory comprising a plurality of unit memories in a two-dimensional array corresponding to a pixel arrangement in the pixel array for storing said analog signals, each unit memory including an analog to digital converter circuit, and

each said analog to digital converter circuit producing a converted digital signal by carrying out analog to digital conversion on a stored analog signal; and

a memory scanning circuit that scans for scanning the AD memory and outputting the converted digital signals from the individual unit memories.

Allowable Subject Matter

2. Claims 1-4, 6-8 are allowed.

Response to Arguments

3. Applicant's arguments filed 2/22/2008 have been fully considered but they are not persuasive.

The inventive concept within the present application is understood and is considered allowable subject matter if defined specifically, as in Claim 1. However, applicant's arguments are not persuasive regarding claims 9-11 because independent claim 9 uses broad language and subsequently examiner interprets the meaning of claim 9 broadly and maintains the original rejection.

Claim 9 defines, inter alia, an AD (analog to digital) memory for *storing* analog signals read from the pixel array and carrying out AD conversion on said analog signals. Since Claim 9 is not further limited as Claim 1 is, then taken with a broad interpretation, Fowler (US 6757018) teaches an AD memory which is seen in Fig. 3. The pixel unit depicted in Fig. 3 can be considered a unit that is *storing* the analog signal converted from light (*from reference number 310),* because it is held for at least a period of time before going to the A/D converter, reference number 314. This unit converts the analog signal to digital. In contrast, although Claim 1 also does not further define "storing" the

analog signal, Claim 1 does define that the AD memory is a plurality of unit memories in a two-dimensional array *corresponding* to a pixel array for storing analog signals, and *each* unit memory including an a/d converter circuit. Claim 1 also defines that each a/d converter circuit produces a converted digital signal by carrying out analog to digital conversion on a stored analog signal. These limitations define the invention more specifically and when taken together can the whole invention be realized over the prior art. Claim 9 as it is currently amended is defined too broadly without the further specific limitations to differentiate it over the prior art. Subsequently, the rejections of the dependent claims are also maintained.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) and Fowler (US 6757018) in view of Pain et al. (US 7268814).

Regarding Claim 9, Gowda teaches a solid-state imaging apparatus comprising: a pixel array, said pixel array comprising a plurality of pixels in a two-dimensional array

(*Fig. 1 reference number 102)*; and an AD circuit for receiving analog signals read from the pixel array and carrying out AD conversion on said analog signals (*Fig. 1 reference number 104)*, the AD circuit comprising a plurality of unit memories in at least a two-dimensional array (*Col 2 Lines 39-45)*. However, Gowda does not teach the AD circuit is and AD memory. However, Fowler teaches an image sensor with each unit containing an ADC, also containing memory, making each unit an AD memory (*as seen in Fig. 3 and Col 4 Lines 44-53)*. Fowler shows that it is well known in the art to associate an ADC and memory component in each unit of an array.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda with that of Fowler to realize an ADC array where each unit performs the ADC and stores it in a memory thereby making each unit an AD memory comprising the units of an AD memory array. It would have been obvious because configurations such as that of Fowler associate the memory in the same unit as the ADC to eliminate transfer of the digitization output of each pixel to a separate memory array. Applying this concept to Gowda would eliminate the need for a separate memory array in order to save time on transferring the output to the separate memory array.

Gowda in view of Fowler do not specifically teach simultaneously carrying out AD conversion, however this is commonly seen in the art.

Pain teaches in Col 4 Lines 29-36 that an ADC in an imaging array can be an ADC array the same size as the pixel array so that all the output signals from the pixels can be digitized in parallel. It would have been obvious to one of ordinary skill in the

art at the time of the invention to modify the teaching of Gowda which teaches an ADC array with one ADC per pixel, to simultaneously perform analog to digital conversion to save on processing time.

Regarding Claim 10, Pain teaches an ADC array can be one ADC per column and also teaches multiple ADC should be used in parallel. If the ADCs are arranged per column, each would be carrying out conversion on a combination of signals from the pixel array, from each column. Each ADC would be converting pixels from each column in parallel. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gowda in view of Fowler, a pixel array with corresponding AD memory array, with that of Pain to realize the parallel processing of ADCs when there is one ADC for more than one pixel. The ADC will receive signals from a combination of pixels and perform digitization in parallel, or simultaneously.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) and Fowler (US 6757018) in view of Pain et al. (US 7268814), further in view of Blerkom et al. (US 6870565).

Regarding Claim 11, Gowda in view of Fowler teach an imaging apparatus with a pixel array and corresponding AD memory array. However they do not teach the AD memory carries out noise removal. Blerkom teaches that integrating ADC array on the

same substrate as the pixel array is a way of removing noise (*Col 2 Lines 10-17).* It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda in view of Fowler and to apply the teaching of Blerkom to perform noise removal on the same place the AD conversion is performed, which is the AD memory array. It would be obvious to carry out noise removal and AD conversion on the signals from the pixel array because combining the ADC and the memory for each unit eliminates noise which would be created when transferring the output of the ADC to a separate memory array.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HSU whose telephone number is (571)270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2622

ARH 6/16/08

/Lin Ye/
Supervisory Patent Examiner, Art Unit 2622